REMARKS

I. Introduction

Applicants would like to thank Examiner Lam for the indication of allowable subject matter recited by claims 5 and 7-26. In response to the Office Action dated December 29, 2004, Applicants have rewritten claims 7 and 16-18 into independent format. Claims 1, 4 and 6 have also been amended so as to further clarify the claimed invention. Support for these amendments can be found, for example, at page 13, line 19 to page 14, line 22 of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1 and 3 Under 35 U.S.C. § 102

Claims 1 and 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 6,430,103 to Nakayama. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1, as amended, recites in-part a plurality of programmable elements, and the operational state of each of the programmable elements being determined during a manufacturing process.

In accordance with one embodiment of the present invention, the separation portion 13 is provided with a plurality of fuse circuits or antifuse circuits. Specifically, if the circuits 131 are fuse circuits (i.e., conductive state) and the logic portion 12B is to be separated from the memory 11 after the semiconductor integrated circuit has undergone the wafer processing, the fuse circuits of the separation portion 13 for the logic portion 12B are disconnected during the

manufacturing process thereof so as to deactivate the logic portion 12B from the memory 11. On the other hand, if the circuits 131 are antifuse circuits (i.e., non-conductive state) and the logic portion 12A is to be connected to the memory 11 after the semiconductor integrated circuit has undergone wafer processing, the antifuse circuits of the separation portion 13 for the logic portion 12A are deactivated during the manufacturing process thereof so as to connect the logic portion 12A to the memory 11. As a result, a logic portion that has become defective during the wafer processing of the semiconductor integrated circuit can be advantageously recovered or replaced to thereby improve the productivity and the yield of the semiconductor integrated circuit.

In the pending rejection, the Examiner relies on Fig. 15 and cols. 14-15 for allegedly disclosing the claimed features. In particular, the Examiner reads the bus switch circuit 55 as the claimed separation portion. As is well known in the art, a switching circuit establishes or changes a connection in a circuit. In the instant case, the bus switch circuit 55 of Nakayama is expressly utilized to selectively create a bus connection between the processors 50-1/50-2 and the main memory 51. As such, the operational state of the bus switch circuit 55 depends on the specific bus transmission required. For example, the bus switch circuit 55 selects the first bus connection state to transmit the access control data output by the processor 50-1 to the main memory 51 so as to enable data input and output between the main memory 51 and the L3 cache memory 1-1 or the processor 50-1. Similarly, the bus switch circuit 55 selects the third bus connection state to transmit the access control data output by the processor 50-1 to the L3 cache memory 1-2 so as to enable data input and output between the L3 cache memory 1-2 and the processor 50-1 or the L3 cache memory 1-1. In other words, the operational state of the bus switch circuit 55 is determined by the desired transmission between the processors, L3 cache

memory and the main memory. In direct contrast, as discussed above, the operational state of the programmable elements is determined during the manufacturing process so that in an event a particular logic portion has become defective during the wafer processing of the semiconductor integrated circuit, the present invention advantageously provides a redundancy-based recovery so that the given semiconductor integrated circuit can still be utilized.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Nakayama fails to disclose or suggest the foregoing claim elements, it is clear that Nakayama does not anticipate claim 1, or any of the claims dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as independent claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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